CLAIMS

What is claimed is:

1. A semiconductor package comprising:

a low-K Si die having front and back surfaces, the low-K Si die including a plurality of layers of low-K material;

a packaging substrate having die and board surfaces;

a heat spreader;

a thermal interface material coupling the heat spreader to the back surface of the low-K Si die, the thermal interface material having a thermal interface material modulus that is higher than or equal to 100 MPa; and

an adhesive coupling the heat spreader to the die surface of the packaging substrate, the adhesive having an adhesive modulus that is lower than or equal to 10 MPa.

2. A semiconductor package as recited in claim 1, wherein the low-K Si die is stably integrated within the semiconductor package such that the reliability of the low-K Si die is not substantially impaired by internal stress of the semiconductor package, the internal stress being created from cycling the temperature of the semiconductor package from -55 °C to 125 °C.

3. A semiconductor package as recited in claim 1, wherein the low-K Si die is an extra low-K Si die including a plurality of layers of extra low-K material.

4. A semiconductor package as recited in claim 1, wherein the layer of low-K material has a thickness of 6 microns or less.

5. A semiconductor package as recited in claim 1, wherein the low-K Si die has a thickness in the range of 19 mil to 28 mil.

6. A semiconductor package as recited in claim 1, wherein the low-K Si die size ranges from 2 mm x 2 mm to 30 mm x 30 mm.

7. A semiconductor package as recited in claim 1, wherein the packaging substrate size ranges up to 45 mm x 45 mm.

8. A semiconductor package as recited in claim 1, wherein the thermal interface material is has a modulus about 400 MPa.

9. A semiconductor package as recited in claim 1, wherein the adhesive has a modulus about 4 MPa.

10. A semiconductor package as recited in claim 1, wherein the front surface of the low-K Si die is electrically and mechanically coupled with the die surface of the packaging substrate.

11. A semiconductor package as recited in claim 10, wherein the low-K Si die includes a plurality of solder bumps on the front surface of the low-K Si die for electrically and mechanically coupling the front surface of the low-K Si die with the die surface of the packaging substrate.

12. A semiconductor package as recited in claim 11, wherein the plurality of solder bumps offset the low-K Si die from the packaging substrate such that a gap is formed in between the front surface of the low-K Si die and the die surface of the packaging substrate.

13. A semiconductor package as recited in claim 12, wherein the gap is filled with an underfill material.

14. A method of forming a semiconductor package comprising:

providing a low-K Si die having front and back surfaces and a packaging substrate having die and board surfaces, the low-K Si die including a plurality of layers of low-K material;

connecting a heat spreader to the back surface of the low-K Si die with a thermal interface material having a modulus that is higher than or equal to 100 MPa; and

connecting the heat spreader to the die surface of the packaging substrate with an adhesive having a modulus that is lower than or equal to 10 MPa.

15. A method of forming a semiconductor package as recited in claim 14, further comprising:

cycling the temperature of the semiconductor package from -55 °C to 125 °C to create internal stress within the semiconductor package, wherein the low-K Si die is stably integrated within the semiconductor package such that the reliability of the low-K Si die is not substantially impaired by the internal stress of the semiconductor package.

16. A method of forming a semiconductor package as recited in claim 14, wherein the low-K Si die is an extra low-K Si die including a plurality of layers of extra low-K material.

17. A method of forming a semiconductor package as recited in claim 14, wherein the layer of low-K material has a thickness of 6 microns or less.

18. A method of forming a semiconductor package as recited in claim 14, wherein the low-K Si die has a thickness in the range of 19 mil to 28 mil.

19. A method of forming a semiconductor package as recited in claim 14, wherein the low-K Si die size ranges from 2 mm x 2 mm to 30 mm x 30 mm.

20. A method of forming a semiconductor package as recited in claim 14, wherein the packaging substrate size ranges up to 45 mm x 45 mm.

21. A method of forming a semiconductor package as recited in claim 14, wherein the thermal interface material is has a modulus about 400 MPa.

22. A method of forming a semiconductor package as recited in claim 14, wherein the adhesive has a modulus about 4 MPa.

23. A method of forming a semiconductor package as recited in claim 14, further comprising:

electrically and mechanically coupling the front surface of the low-K Si die with the die surface of the packaging substrate.

24. A method of forming a semiconductor package as recited in claim 23, wherein the low-K Si die includes a plurality of solder bumps on the front surface of the low-K Si die for electrically and mechanically coupling the front surface of the low-K Si die with the die surface of the packaging substrate.

25. A method of forming a semiconductor package as recited in claim 24, wherein the plurality of solder bumps offset the low-K Si die from the packaging substrate such that a gap is formed in between the front surface of the low-K Si die and the die surface of the packaging substrate.

26. A semiconductor package, comprising:

a low-K Si die having front and back surfaces and a packaging substrate having die and board surfaces, the low-K Si die including a plurality of layers of low-K material;

means for electrically and mechanically coupling the front surface of the low-K Si die with the die surface of the packaging substrate;

means for connecting a heat spreader to the back surface of the low-K Si die with a thermal interface material having a modulus that is higher than or equal to 100 MPa; and

means for connecting the heat spreader to the die surface of the packaging substrate with an adhesive having a modulus that is lower than or equal to 10 MPa.